

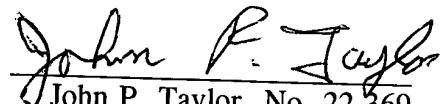
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REMARKS

Original claims 1-14 have been cancelled and new claims 18-19 have been added. Claims 15-19 are now in the application.

Respectfully Submitted,



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VERSION WITH MARKINGS TO SHOW CHANGES MADEIn the Specification:

Please replace the paragraph beginning at page 3, line 16, with the following rewritten paragraph:

--~~Copending application Docket No. A3 4318, entitled "LOW DIELECTRIC CONSTANT SILICON OXIDE BASED DIELECTRIC LAYER FOR INTEGRATED CIRCUIT STRUCTURES HAVING IMPROVED COMPATIBILITY WITH VIA FILLER MATERIALS, AND METHOD OF MAKING SAME", was filed by one of us with others on the same date as this application and is assigned to the same assignee as this application. The subject matter of Docket No. A3 4318 is hereby incorporated by reference.~~ In one embodiment in the aforementioned Serial No. 09/426,061 ~~that application~~, low k silicon oxide dielectric material having a high carbon doping level is formed in the high aspect regions between closely spaced apart metal lines and then a second layer comprising a low k silicon oxide dielectric material having a lower carbon content is then deposited over the first layer and the metal lines. However, since both layers are formed by the Trikon process, the deposition rate does not radically change.--

Please replace the paragraph beginning at page 3, line 27, with the following rewritten paragraph:

--~~Copending application Docket No. 99-060 entitled "INTEGRATED CIRCUIT STRUCTURE HAVING LOW DIELECTRIC CONSTANT MATERIAL AND HAVING SILICON OXYNITRIDE CAPS OVER CLOSELY SPACED APART METAL LINES" was also filed by one of us with others on the same date as this application and is assigned to the same assignee as this application. The subject matter of Docket No. 99-060 is also hereby incorporated by reference. In the aforementioned Serial No. 09/425,552 that application, a layer of silicon oxynitride (SiON) is formed over the top surface of the metal lines to serve as an anti-reflective coating (ARC), a hard mask for the formation of the metal lines, and a buffer layer for chemical mechanical polishing (CMP). Low k silicon oxide dielectric material having a high carbon doping level is then formed in the high aspect regions between closely spaced apart metal lines up to the level of the silicon oxynitride. CMP is then applied to planarize the upper surface of the low k carbon-doped silicon oxide dielectric layer, using the SiON layer as an etch stop, i.e., to bring the level of the void-free low k silicon oxide dielectric layer even with the top of the SiON layer. A conventional (non-low k) layer of silicon oxide dielectric material is then deposited by plasma enhanced chemical vapor deposition (PECVD) over the low k layer and the SiON layer. A via is then cut through the second dielectric layer and the SiON to the top of the metal line. Since the via never contacts the low k layer between the metal lines, via poisoning due to exposure of the low k layer by the via does not occur.--~~

Please replace the paragraph beginning at page 8, line 7, with the following rewritten paragraph:

--Such void-free low k silicon oxide dielectric material may be deposited by reacting hydrogen peroxide with a carbon-substituted silane such as methyl silane, as described in Dobson U.S. Patent No. 5,874,367, the subject matter of which is hereby incorporated by reference. The void-free low k silicon oxide dielectric material may also be deposited by reacting a mild oxidant such as hydrogen peroxide with the carbon-substituted silane materials disclosed in Aronowitz et al. U.S. Patent 6,303,047 Serial No. 09/274,457, filed on March 22, 1999, and assigned to the assignee of this application, the subject matter of which is also hereby incorporated by reference.--